1. A method of forming multiple gate insulator layers on a semiconductor substrate, comprising the steps of:

forming a first insulator layer on said semiconductor substrate;

forming a photoresist shape on a first section of said first insulator layer;

removing second section of said first insulator layer exposing a bare first section of said semiconductor substrate;

performing a first photoresist removal procedure resulting in partial removal of said photoresist shape and forming a second insulator layer on said bare first section of said semiconductor substrate;

performing a second photoresist removal procedure completely removing said photoresist shape;

performing a procedure to convert said first insulator layer located on a second section of said semiconductor substrate, to a first gate insulator layer, and to convert said second insulator layer to a second gate insulator layer, wherein the thickness of said first gate insulator is different than the thickness of said second gate insulator layer; and forming a first conductive gate structure on said first gate insulator layer and forming a second conductive gate structure on said second gate insulator layer.

2. The method of claim 1, wherein said first insulator layer is a silicon dioxide layer, at a thickness between about 10 to 200 Angstroms.

3. The method of claim 1, wherein removal of said second section of said first insulator layer is accomplished via use of a buffered hydrofluoric (BHF) acid solution.

4. The method of claim 1, wherein said first photoresist removal procedure is performed using ozone water.

5. The method of claim 1, wherein said second insulator layer formed on said second section of said semiconductor substrate, is a silicon oxide layer at a thickness between about 8 to 10 Angstroms.

6. The method of claim 1, wherein said second photoresist removal procedure is performed using a sulfuric acid - hydrogen peroxide mixture (SPM).

7. The method of claim 1, wherein said second photoresist removal procedure is performed at a temperature between about 110 to 150°C.

8. The method of claim 1, wherein said procedure used to convert said first insulator layer and said second insulator layer to gate insulator layers is an oxidation procedure, performed in an oxygen - steam ambient.

9. The method of claim 1, wherein said procedure used to convert said first insulator layer and said second insulator layer to gate insulator layers is an oxidation procedure, performed at a temperature between about 800 to 1050° C.

10. The method of claim 1, wherein said first gate insulator layer is a silicon dioxide layer, at a thickness between about 15 to 200 Angstroms.

11. The method of claim 1, wherein said second gate insulator layer is a silicon dioxide layer, at a thickness between about 10 to 100 Angstroms.

12. The method of claim 1, wherein said first conductive gate structure and said second conductive gate structure are comprised of doped polysilicon.

13. The method of claim 1, wherein said first conductive gate structure and said second conductive gate structure are comprised of metal silicide.

14. A method of forming a semiconductor device on a semiconductor substrate featuring multiple gate insulator thicknesses, comprising the steps of:

forming a first silicon oxide layer on entire surface of said semiconductor substrate;

forming a photoresist shape on a first section of said first silicon oxide layer, in a region overlying a first section of said semiconductor substrate;

removing second section of said first silicon oxide layer exposing a bare second section of said semiconductor substrate;

performing an ozone containing mixture procedure to partially remove said photoresist shape and to form a second silicon oxide layer on said bare second section of said semiconductor substrate;

performing a sulfuric acid - hydrogen peroxide mixture (SPM) procedure, to completely remove said photoresist shape; and

performing an oxidation procedure to convert said first silicon oxide layer to a first gate insulator layer on said first section of said semiconductor substrate, and to convert said second silicon oxide layer to a second gate insulator layer, wherein the thickness of said first gate insulator is greater than the thickness of said second gate insulator layer; and

forming a first conductive gate structure on said first gate insulator layer and forming second conductive gate structure on said second gate insulator layer.

15. The method of claim 14, wherein said first silicon oxide layer is a silicon dioxide layer, at a thickness between about 10 to 200 Angstroms.

16. The method of claim 14, wherein removal of said second section of said first silicon oxide layer is accomplished via use of a buffered hydrofluoric (BHF) acid solution.

17. The method of claim 14, wherein removal of said second section of said first silicon oxide layer is accomplished via dry etching procedures using CHF_3 as a selective etchant for said first silicon oxide layer.

18. The method of claim 14, wherein ozone water procedure is performed at a temperature between about 20 to 50° C.

19. The method of claim 14, wherein the thickness of said second silicon oxide layer formed on said second section of said semiconductor substrate, is between about 8 to 10 Angstroms.

20. The method of claim 14, wherein said sulfuric acid - hydrogen peroxide mixture (SPM) procedure is performed at a temperature between about 110 to 150° C.

21. The method of claim 14, wherein said oxidation procedure is performed at a temperature between about 800 to 1050° C.

22. The method of claim 14, wherein said first gate insulator layer is a silicon dioxide layer, at a thickness between about 15 to 200 Angstroms.

23. The method of claim 14, wherein said second gate insulator layer is a silicon dioxide layer, at a thickness between about 10 to 100 Angstroms.

24. The method of claim 14, wherein said first conductive gate structure and said second conductive gate structure are comprised of doped polysilicon.

25. The method of claim 14, wherein said first conductive gate structure and said second conductive gate structure are comprised of metal silicide.